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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/542,783

Filing Date: April 04, 2000

Appellant(s): WHITMAN ET AL.

Brick G. Power
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed September 29, 2005 appealing from the Office action mailed May 12, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

U.S. Application Serial No. 09/944,230.

U.S. Application Serial No. 09/997,019.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon the rejection of claims under appeal.

U.S. Patent 6,046,083	Lin et al.	4-2000
U.S. Patent 6,117,486	Yoshihara	9-2000
U.S. Patent 6,278,153	Kikuchi et al.	8-2001
U.S. Patent 6,326,282	Park et al.	12-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

a. **Claims 1, 2, 8, 9, 11, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Kikuchi et al. (US/6,278,153).**

Re claim 1, Kikuchi et al. disclose a method for disposing a material on a semiconductor device structure comprising: providing a semiconductor device structure (see Fig. 6D) including a surface (23 24 25 26) and at least one recess (23a) formed in the surface; disposing the material (20) on the surface (23 24 25 26) so as to substantially fill at least one recess (23a) and the material (20) covering the surface having a thickness less than a depth of said at least one recess (23a) without subsequently removing the material (20) from the surface, an upper surface of at least a portion of said material (20) over or within said at least one recess being substantially planar (23 24 25 26) (see Figs. 6A-6D; 10A-10E and 13A-13E;).

Re claim 2, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including disposing the material so as to substantially fill the at least one recess without substantially covering said surface (see Figs. 6A-6D; 10A-10E and 13A-13E;).

Re claim 8, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including upon exposing the material disposed over an entirety of said semiconductor device structure to an etchant, the material covering said surface is substantially removed therefrom, while the material located in said at least one recess substantially fills said at least one recess (see Figs. 6A-6D; 10A-10E and 13A-13E).

Re claim 9, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation wherein said providing said semiconductor device structure comprises providing a stacked capacitor structure with said at least one recess comprising at least one container formed in an insulator layer of said stacked capacitor structure, said surface and said at least one container being lined with a conductive material (see Figs. 6A-6D; 10A-10E; 13A-13E)

Re claim 11 as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation wherein said disposing the material comprises disposing a mask material over said semiconductor device structure (see Fig. 6A-6D; 10A-10E; 13A-13E).

Re claims 16 and 17, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation providing a semiconductor device structure having a surface with at least one dual damascene trench recessed therein and a layer of conductive material, with a non-planar surface disposed in said at least one dual damascene trench and at least partially covering said surface and disposing a stress buffer over said layer of conductive material, said

stress buffer having a substantially planar surface without removing material thereof following said disposing (see Figs. 14A-14D).

b. **Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. (US/6,278,153) in view of Yoshihara (US/6,117,486).**

Re claims 3-7, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation applying the material to the surface of the semiconductor device structure spinning the semiconductor device structure (see Kikuchi et al. Figs. 6A-6D; 10A-10E and 13A-13E). However, Kikuchi et al. do not disclose decreasing a rate of the spinning while permitting the material to at least partially cure and gradually increasing the rate of the spinning.

Yoshihara discloses applying the material to the surface of the semiconductor device structure spinning the semiconductor device structure both decreasing rate of spinning and while allowing the material to cure gradually increasing the rate of spinning; exposing the material to a soft balling temperature ; spinning rate of 1000 and 100 rpm (see Figs. 10 and Col. 13, lines 25-44). As Yoshihara discloses the method provided forming of resist film on the semiconductor wafer at predetermined and uniform thickness.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Kikuchi et al. reference with spinning the semiconductor device structure both decreasing rate of spinning and while allowing the material to cure gradually increasing the rate of spinning as taught by Yoshihara because the

method would have provided to form a resist film on the semiconductor wafer at predetermined and uniform thickness.

c. **Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. (US/6,278,153) in view of Lin et al. (US/6,046,083).**

Re claim 10, as applied to claim 9 above, Kikuchi et al. disclose all the claimed limitations including forming of stacked capacitor structure having conductive layer. Although it is well-known in the art Kikuchi et al. do not disclose doped HSG.

Lin et al. disclose providing said semiconductor device structure having a stacked capacitor structure with the surface and at least one container being lined, with doped hemispherical grain polysilicon (see Figs. 7 and 8).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Kikuchi et al. reference with doped HSG as taught by Lin et al. because the device performance would have been enhanced (see Lin et al. Col. 1, lines 59-67 through Col. 2, lines 1-14).

d. **Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. (US/6,278,153) in view of Park et al. (US/6,326,282).**

Re claim 12, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation except providing a shallow trench isolation structure with at

least one recess comprising at least one trench formed in a surface of the shallow trench isolation structure.

Park et al. disclose forming of a shallow trench isolation structure with at least one recess comprising at least one trench formed in a surface of the shallow trench isolation structure in order to form an isolation region between the device elements (see Figs. 2B-2E).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Kikuchi et al. reference with shallow trench isolation structure as taught by Park et al. because the shallow trench isolation structure would have provided isolation region between device elements in the substrate.

Re claim 13, as applied to claim 12 above, both Kikuchi et al. and Park et al. in combination disclose all the claimed limitations including the limitation wherein said disposing the material comprises disposing a mask material over said shallow trench isolation structure (see Park et al. Figs. 2B-2E).

Re claim 14, as applied to claim 12 above, both Kikuchi et al. and Park et al. in combination disclose all the claimed limitations including the limitation wherein said providing said shallow trench isolation structure comprises providing said shallow trench isolation structure with an insulator layer substantially filling said at least one trench and covering said surface see Park et al. Figs. 2B-2E).

Re claim 15, as applied to claim 14 above, both Kikuchi et al. and Park et al. in combination disclose all the claimed limitations including the limitation wherein said disposing the material comprises disposing a stress buffer over said insulator layer, said stress buffer

having a substantially planar surface without removing material thereof following said disposing see Park et al. Figs. 2B-2E).

(10) Response to Argument

Appellants' argument filed on September 29, 2005 have been fully considered but they are not persuasive.

I.

A.

With respect to claims 1, 2, 8, 9, 11, 16, and 17, Appellants argue that "Kikuchi does not anticipate a method that includes disposing material such a way that an upper surface at least a portion of [the] material over or within...at least one recess [is] substantially planar...," (see Appellants argument in Pages 9-12).

In response to Appellants' argument, it is respectfully submitted that such argument is not commensurate with the scope of the claims. It is respectfully submitted that Kikuchi et al. '153 anticipates all the limitations of Claims 1, 2, 8, 9, 11, 16, and 17 of the instant application as applied in Paragraph 9(a) herein above.

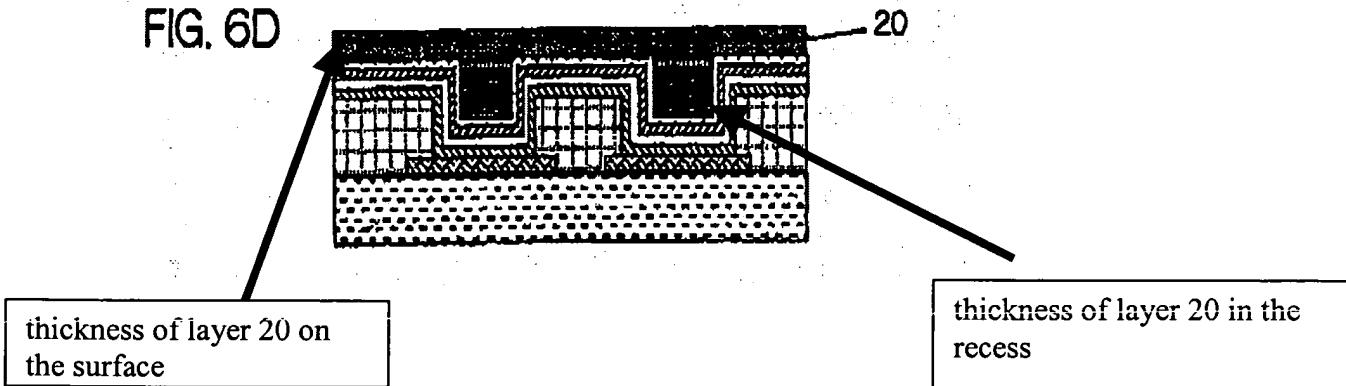
With respect to claim 1, Kikuchi et al. disclose a method for disposing a material on a semiconductor device structure comprising: providing a semiconductor device structure (see Fig. 6D) including a surface (23 24 25 26) and at least one recess (23a) formed in the surface; disposing the material (i.e., a resist layer) (20) on the surface (23 24 25 26) so as to substantially fill at least one recess (23a) and the material (20) covering the surface having a thickness less than a depth of the at least one recess (23a) without subsequently removing the material (20)

from the surface, an upper surface of at least a portion of said material (20) over or within the at least one recess being substantially planar (see Figs. 6A-6D; 10A-10E and 13A-13E; 16A-16F).

Since there is no quantitative dimensional range can be found in the Appellants disclosure, Appellants' argument that "Kikuchi et al. '153 drawings are not to scale" has no merit because Applicants' own drawings are not in scale also. As claimed in claim 1, Figs. 2 and 3 provide support for the instant application and Figs. 2 and 3 are not in scale. The only interpretation to the claim language in order to determine the scope of Appellants' claimed invention by visual examination of the top material layer 18 relative to the depth of the recess and on the top surface of the layer 16. In this respect, Kikuchi et al. '153 appears to teach the claimed subject matter as depicted in Fig. 6D.

For example, as depicted in Fig. 6D below, Kikuchi et al. '153 appear to show the thickness of layer 20 at the surface is lower than that of similar to Figs. 2 and 3 of the instant application .

FIG. 6D



In addition, Fig. 6D appears to show “substantially planar” surface of the resist layer 20 on the surface which substantially fill the recess 23a. Kikuchi et al. '153 also disclose in the specification spin-coating process, i.e., a well-known process to one having ordinary skill in the art to deposit resist layer and to planarize the layer, which by the way same process is used in the instant application for the purpose of achieving planar surface. The following disclosed by Kikuchi et al. '153: “as illustrated in FIG. 6D, resist 20 is deposited over the third electrically conductive thin layer 27. If the resist 20 composed of liquid material, the liquid material is deposited on the third electrically conductive layer 27 by spin-coating, die-coating, curtain-coating or printing (see . Kikuchi et al. '153 Col. 17, lines 62-66). The purpose of spin-coating during deposition of the resist layer, as well-known to one of ordinary skill in the art, is to form a resist layer having a planar surface. As the term implies, spin coating removes excess material as result of spinning of the wafer during coating operation. Therefore, Kikuchi et al. '153 as shown in Fig. 6D explicitly or implicitly teach depositing of a material 20 having “substantially planar” surface on a surface.

Appellants further argue that “Kikuchi lacks any inherent description that method described therein results in a layer resist layer 20 that includes a portion over within a recess with a planar surface...” In response to Appellants’ argument, as shown in Fig. 6D and other drawings, such a, in Figs 10C, 13D, and 15D the resist layer appears to have uniform-planar every region of the surface below. Further in response to Appellants’, it is respectfully submitted that nothing in claim 1 specifies quantitative or qualitative measurement or **degree of planarization**. In addition, claim 1 does not recite how **planarization** process is conducted that can be different form that of the Kikuchi et al. '153 reference. As a matter of fact, claim 1 recites

“the material over or within the at least of one recess being substantially planar.” Kikuchi et al. ’153 appear to disclose a “substantial planar” resist layer 20 as depicted in Fig. 6D that resulted from spin coating process (i.e., a similar process as of the spin coating process of the instant application).

In this case, claims are given their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

With respect to claim 2, appellants further argued that “Kikuchi neither expressly nor inherently describes *disposing* a material on a surface of a semiconductor device structure and within recesses thereof so as to substantially fill the recesses *without substantially covering the surface, . . .*”

In response to the Appellants’ argument, it is respectfully submitted Kikuchi et al. ’153 teach all the claimed limitations of claim 2.

In light of the supporting disclosure, claim 2 is interpreted in view of Figs. 2 and 3 of the instant application. For illustrative purpose, Figs. 2 and 3 are reproduced below.

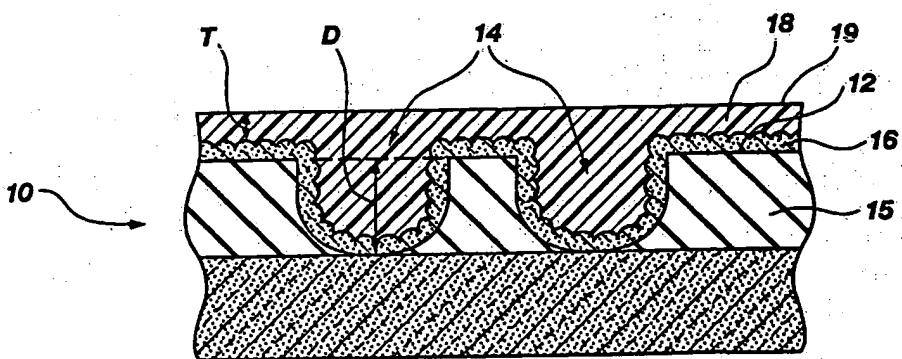


Fig. 2

As depicted in Fig. 2 above, the material layer 18 is disposed over a surface 12 to substantially fill the recess (container) 14 (see the instant application specification in Page 12, paragraph [0038]). As recited in claim 2, “wherein said disposing comprises disposing said material so as substantially fill said at least one recess without substantially without substantially covering said surface” is interpreted in conjunction with Fig. 3. After the material layer 18 (i.e., the resist layer) deposited to fill the recess 14 and cover the surface 12 as shown in Fig. 2 above, the material layer 18 (i.e., the resist layer) is removed from the surface (i.e., *disposing* a material on a surface of a semiconductor device structure and within recesses thereof so as to substantially fill the recesses *without substantially covering the surface*) during subsequent process as shown in Fig. 3 below (see also the instant application specification page 14, paragraph 0041).

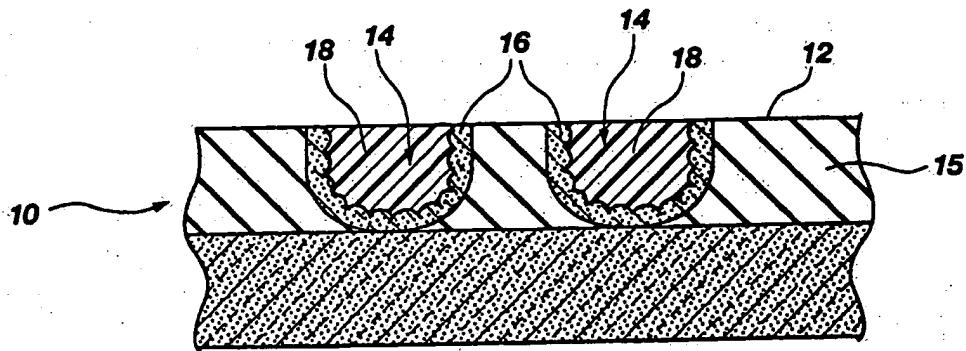


Fig. 3

In addition, there is no selective deposition process disclosed in Appellants' disclosure or in the rejected claims that would lead one of ordinary skill in the art to a different interpretation.

Similarly, Kikuchi et al. '153 disclosure, as depicted in Figs. 6E and 6F or 16D-16F below, is consistent with claim 2 and Figs. 2 and 3 of the instant application.

FIG. 6E

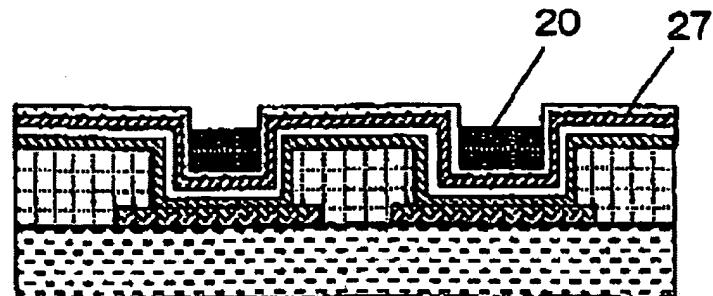


FIG. 6F

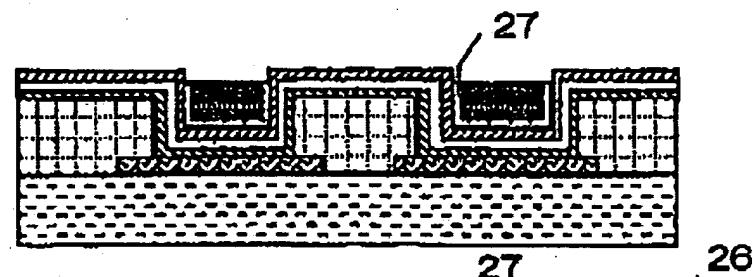


FIG. 16D

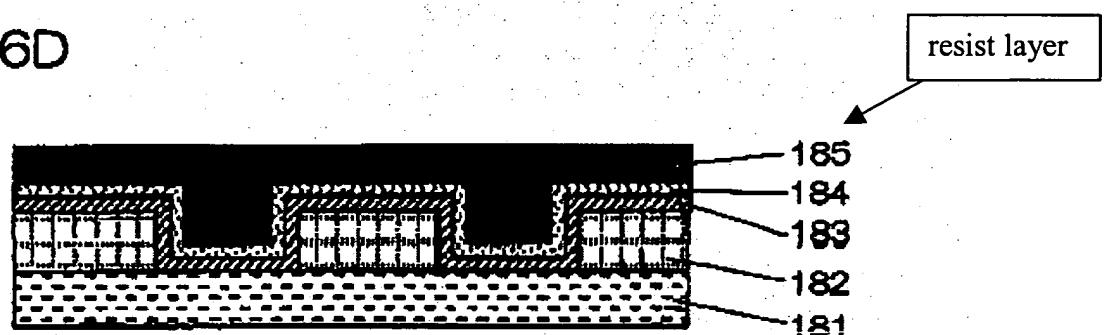


FIG. 16E

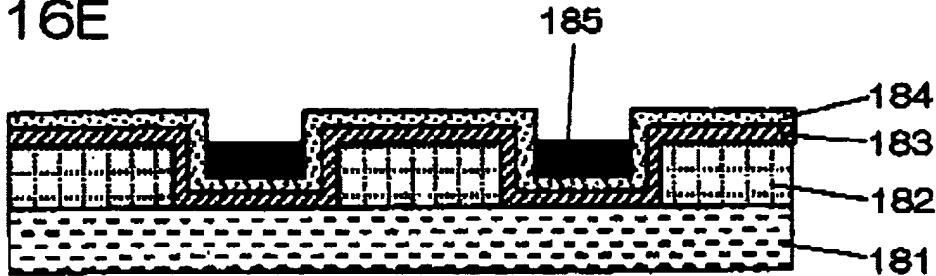
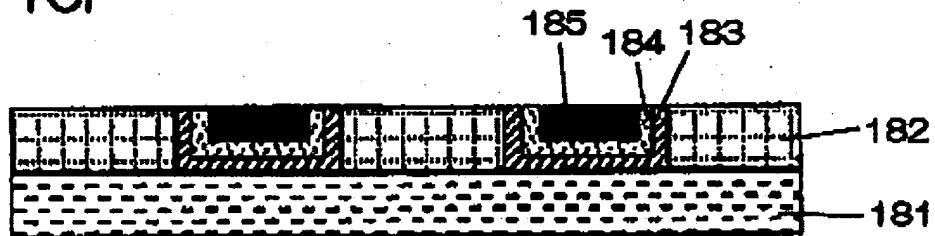


FIG. 16F



Hence, Appellants contention that “Kikuchi neither expressly nor inherently describes disposing a material on a surface of a semiconductor device structure and within recesses thereof so as to substantially fill the recesses without substantially covering the surface...” has no merit because the rejected claim is consistent with Kikuchi et al. '153 disclosure as shown in Fig. 16F as result of the subsequent steps. In other word, material layer 184 formed within the recess after subsequent processes without being formed on the surface 182.

Furthermore, claims are given their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not

read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Therefore, the rejection of claims 1, 2, 8, 9, 11, 16 and 17 under 35 U.S.C. § 102 is deemed proper.

B.

With respect claims 3-7, appellants' argue that (see the brief in Pages 13-16) “neither Kikuchi, Yoshihara, nor knowledge available to one ordinarily skilled in the art would have motivated one of ordinary skill in the art to combine teachings from Kikuchi with teachings from Yoshihara to arrive at the inventions to which claims 3-7 are drawn...”

In response to Appellants' argument, it is respectfully submitted that the combination of Kikuchi et al. '153 and Yoshihara '486 teach all the limitations of Claims 3-7 of the instant application as applied in Paragraph 9(b) herein above.

The combination of Kikuchi et al. '153 and Yoshihara '486 discloses applying the material to the surface of the semiconductor device structure, spinning the semiconductor device structure and decreasing rate of spinning while allowing the material to cure gradually, and finally increasing the rate of spinning; exposing the material to a soft balling temperature; spinning rate of 1000 and 100 rpm (see Yoshihara '486 Figs. 10 and Col. 13, lines 25-44).

Both Kikuchi et al. '153 and Yoshihara '486 teachings are directed to coating of material (i.e., resist coating) on a substrate for the purpose of fabricating semiconductor device. Therefore, the teachings of Kikuchi et al. '153 and Yoshihara '486 are analogous. It would have been within the scope of ordinary skill in the art to combine the teachings of Kikuchi et al. '153 and Yoshihara '486 in order to modify spin coating process of Kikuchi et al. '153 by adjusting

the spinning rate (rpm) according to the teachings of Yoshihara '486 because one having ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods for spin coating process as disclosed by Yoshihara '486. In addition, the rational to combine (i.e., to form a resist film on the semiconductor wafer at predetermined and uniform thickness) the references can be found in Yoshihara '486 Col. 13, line 26 - Col. 14, line 67. The strongest rationale for combining references is a recognition, expressly or impliedly in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been produced by their combination. See *In re Sernaker*, 702 F.2d 989, 994-95, 217 USPQ 1, 5-6 (Fed. Cir. 1983).

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

C.

Pertaining to appellants' argument on Page 16, with respect claim 10, i.e., "claim 10 should be allowable because claim 1 is allowable..." it is respectfully submitted that such an argument is not convincing because claim 1 is not allowable for the reasons indicated in Paragraph 10(A) above. It is respectfully submitted that the combination of Kikuchi et al. '153 and Lin et al. '083 teach all the limitations of Claim 10 of the instant application as applied in Paragraph 9(c) herein above.

Both Kikuchi et al. '153 and Lin et al. '083 teachings are directed to depositing semiconductor thin films over the semiconductor substrate for purpose of fabricating a semiconductor device, particularly, semiconductor stacked capacitor device. Therefore, the

teachings of Kikuchi et al. '153 and Lin et al. '083 are analogous. It would have been within the scope of ordinary skill in the art to combine the teachings of Kikuchi et al. '153 and Lin et al. '083 in order to increase the surface area of the capacitance the capacitor of Kikuchi et al. '153 by using doped hemispherical grain polysilicon according to the teachings of Lin et al. '083. One having ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods for increasing the surface area of the capacitor by utilizing doped hemispherical grain polysilicon as applied by Lin et al. '083.

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

D.

Pertaining to Appellants' argument on Page 16, with respect claims 12-15, i.e., "claims 12-15 should be allowable because claim 1 is allowable...," it is respectfully submitted that claims 12-15 should fall with claim 1 for the reasons indict in Paragraph 10(A) above. It is respectfully submitted that the combination of Kikuchi et al. '153 and Park et al. '282 teach all the limitations of Claims 12-15 of the instant application as applied in Paragraph 9(d) herein above.

Both Kikuchi et al. '153 and Park et al. '282 teachings are directed to fabricating a semiconductor active devices on a semiconductor substrate. Therefore, the teachings of Kikuchi et al. '153 and Park et al. '282 are directed to analogous art. It would have been within the scope of ordinary skill in the art to combine the teachings of Kikuchi et al. '153 and Park et al. '282 in order to provide isolation between different transistor or capacitor areas of Kikuchi et al. '153 by using the shallow trench isolation (SIT) as taught by Park et al. '282 because one

having ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods for electrically isolating one device from another.

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Finally, it is respectfully submitted that the recent ruling of the Federal Circuit Court, in *Playtex Products Inc. v. Procter & Gamble Co.*, 73 USPQ2D 2010, 2015 (CFC 2005), i.e., with respect to the meaning of "substantial" or "substantially planar" (i.e., as described in the Appellants' own specification to the scope and the meaning of "planar surface" as claimed in the claims), should be considered in determining of patentability of the instant application claimed invention.

Respectfully submitted,

Brook Kebede
BROOK KEBEDE
PRIMARY EXAMINER

Appeal conference has been held on December 8, 2005. The Conferees listed herein below.

1. Drew A. Dunn, Chair Person and SPE Art Unit 2872 *DD*
2. Matthew S. Smith, SPE Art Unit 2823 *MS*
4. Brook Kebede, Examiner Art Unit 2823 *BK 10/05*

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December 10, 2005

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